Technical Note

Trends and Issues in Ultra-High-Speed Transmission Technologies

For the implementation of 100 GbE/40 GbE and long haul transmission by optical modulation

MP1800A

Signal Quality Analyzer

Trends and Issues in Ultra-High-Speed Transmission Technologies

1. Market Trends

The daily and rapid spread of the broadband environment is led by FFTx. In these circumstances, core networks are starting to see a genuine transition from 10 Gbps to 40 Gbps. In particular, the focus is on traffic between Internet Exchanges (IXs) and Internet Service Providers (ISPs) and the data rate at the Japan IX (JPIX) now exceeds 100 Gbps, while the world's busiest IX in Amsterdam (AMSIX) exceeds 400 Gbps.

To resolve these types of bottlenecks in core networks, in July 2006, the IEEE started work on examining the 100 GbE standard under the auspices of the HSSG (High Speed Study Group); work started in November 2007 on the IEEE802.3ba standard with the aim of implementation in June 2010. The group is investigating a 100 GbE standard for connecting IXs, ISPs, and Contents Service Providers (CSPs) as well as a 40 GbE standard for connecting servers, etc., in data centers. However, these discussions are not just about standards for LANs using 100 and 40 GbE, but also cover OTN (Optical Transport Unit: OTU3, OTU4) ITU-T SG15 standards for WANs supporting long haul transmissions. R&D into and rollout of 40 Gbps, long haul transmission systems, especially undersea cables, using previously commercialized SDH/SONET/OTN transmission technologies is already starting.

In addition to explaining the latest technology trends from the viewpoint of a measuring instrument maker, this article also describes the important measurement items.

2. Standards Trends

2.1 IEEE Transition to 40/100 GbE Standard

IEEE802.3ba discusses methods for achieving 100 GbE and 40 GbE. 100 GbE is mainly targeted at connections within IXs and between IXs and ISPs, so 40 GbE is being examined for internal connections between servers and storage where bandwidth up to 100 GbE is not required and for equipment interconnects. The following figure shows the topology currently under discussion.

40 GbE	≥10 km on SMF
	≥100 m on OM3 MMF
	≥10 m over copper cable
	≥1 m over backplane
100 GbE	≥40 km on SMF
	≥10 km on SMF
	≥100 m on OM3 MMF
	≥10 m over copper cable

In addition, the 40 GbE and 100 GbE layers are described as shown below in IEEE 802.3ab Draft 1.0.

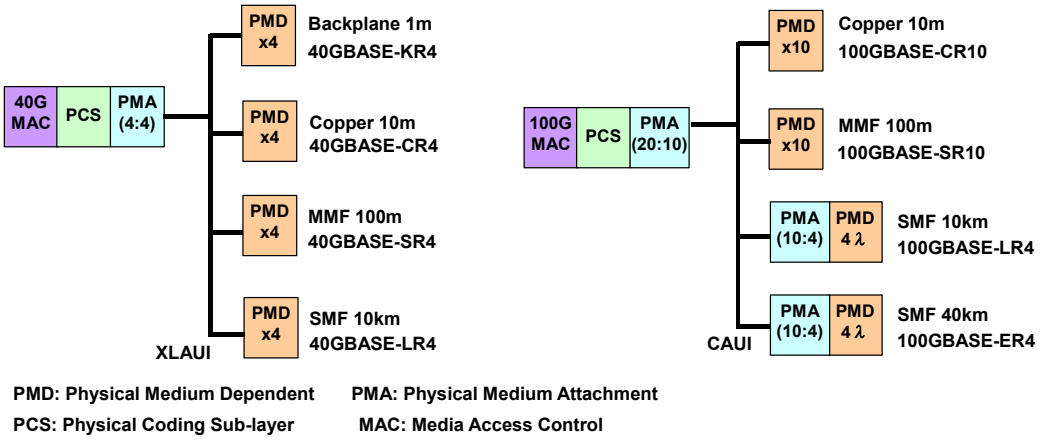

Figure 1. 40 GbE/100 GbE Topologies

From the above, the Media Dependent Interface (MDI) connecting the PMD and network side is being discussed as four parallel transmission lanes each of 10 Gbps for 40 GbE and either 10 parallel transmission lanes of 10 GbE or 4 parallel transmission lanes each of 25 Gbps for 100 GbE. Additionally, the PMD–PMA interface is composed of 4 lanes x 10 Gbps called XLAUI for 40 GbE and 10 lanes x 10 Gbps called CAUI for 100 GbE. Moreover, the optical modules used by 100GBASE-LR4 and 100GBASE-ER4 are expected to be standardized as CFP (100G Form-factor Pluggable) in the MSA (Multi Source Agreement).

2.2 ITU-T, OIF and Trend in 40G Long-Distance Transmission

Although 100 GbE and 40 GbE are defined by IEEE as the standards for the LAN side, ITU-T is also discussing encapsulation of 40 GbE and 100 GbE in OTU4 for the related WAN side. In September 2008, ITU-T SG15/Q11 selected 111.89973 Gbps as the OTU4 bit rate.

Furthermore, in line with these trends, the Optical Internetworking Forum (OIF) seems likely to settle on the 100G long distance DWDM transmission Implementation Agreement (OIF 2008.125.04) using DP-QPSK (Dual Polarization–Quadrature Phase Shift Keying) as the phase modulation method for transmission systems exceeding 100 Gbps in late 2009. (DP-QPSK is also called PM-QPSK when using the PM abbreviation for Polarization Multiplexing instead of Dual Polarization).

Some core networks are already in commercial operation at 40 Gbps but the more widespread standards are still 10 and 2.5 Gbps. Around 2000, communications vendors and carriers started examining long haul transmission using either 2.5 or 10 Gbps WDM, or 40-Gbps serial two make efficient use of bandwidths higher than 40 Gbps. Realistically, not only are there technical issues with PMD, CD, and fiber non-linearity, there are still cost issues about how to overcome them. However, due to the current explosive growth in the spread of 10 GbE traffic between IXs and ISPs, long haul core network traffic is also facing the need to genuinely support 40 Gbps.

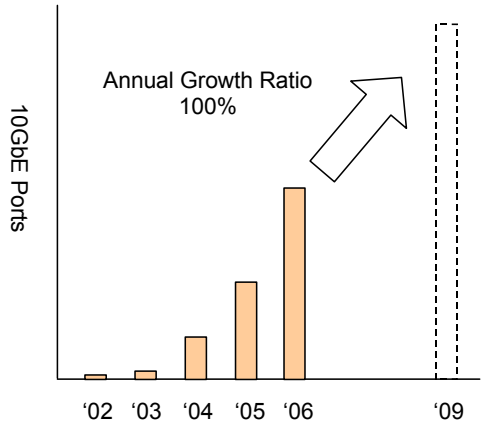

Figure 2. Trend in 10-Gbps Port Count

Businesses currently supporting 40-Gbps long haul transmissions are developing various phase modulation methods such as DQPSK (Differential Quadrature Phase Shift Keying) and DP-QPSK instead of using On/Off modulation to perform data transfer. As a result, the previous problems with PMD, CD and non-linearity that adversely impacted 40-Gbps serial transmissions are expected to be largely solved. The next section outlines these modulation methods.

3. Outline of Modulation Methods

Generally, optical transmission methods use strong modulation with NRZ and RZ, which is commonly called Amplitude Shift Keying (ASK). In the most basic NRZ scheme, the optical signal is switched ON (light emitted) and OFF (light extinguished) to transfer data using a simple binary 0/1 code. The RZ scheme uses the same ON/OFF change to transfer information but in the RZ method, the pulse width at ON is half that in the NRZ scheme. As a result, since the optical power per bit is approximately halved, the impact of non-linearity is reduced. In an optical fiber, the index of refraction (IOR) varies (called non-linearity) with changes in power, meaning as the optical signal goes ON/OFF. When the optical power changes greatly at ON/OFF switching, the IOR changes greatly too,

causing increased degradation in the optical signal after transmission through the fiber. On the other hand, since the optical power in the RZ scheme is twice that in the NRZ scheme, the average optical power is the same as the NRZ scheme, so an improvement in the SNR (signal to noise ratio), can be expected.
By using an RZ transmission signal, the average power drops so the effect of non-linearity drops too, but on the other hand, SNR at the Rx side improves as optical power rises, so a choice is possible.
However, because the pulse width is halved in the RZ scheme and high frequency components are included in the signal, the required frequency band becomes wider. As a result, when multiplexing high-density wavelengths such as DWDM, interference occurs easily between wavelengths, which is a disadvantage.

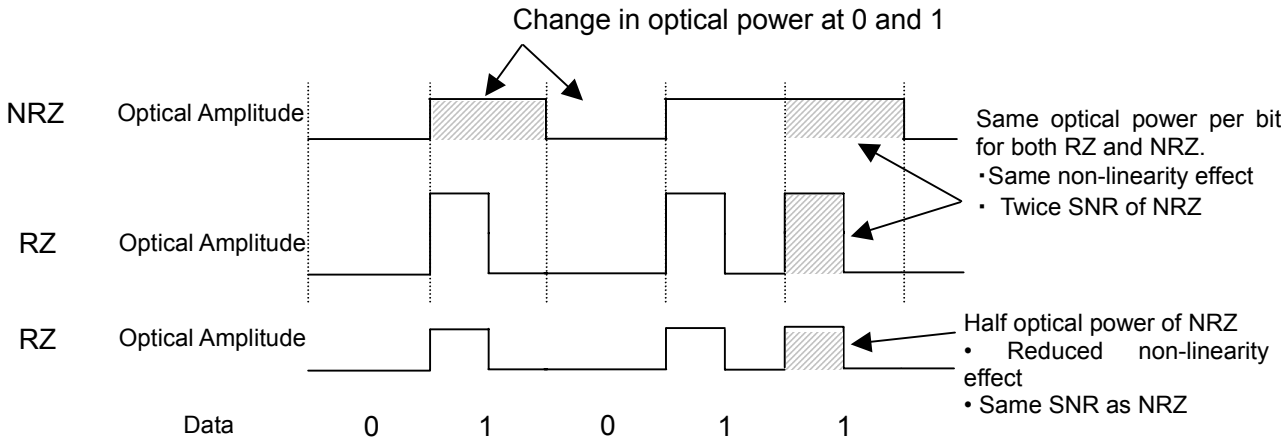

Figure 3. NRZ and RZ Transmissions

Phase Shift Keying (PSK) transmission methods, such as DPSK and DQPSK, eliminate the causes of degraded signal transmissions due to non-linearity. In DPSK, instead of transferring data by switching the optical signal ON/OFF, the optical signal is always on and the information is carried on the shifting signal phase, but because the power is always on, changes in IOR are removed, eliminating the cause of non-linearity.

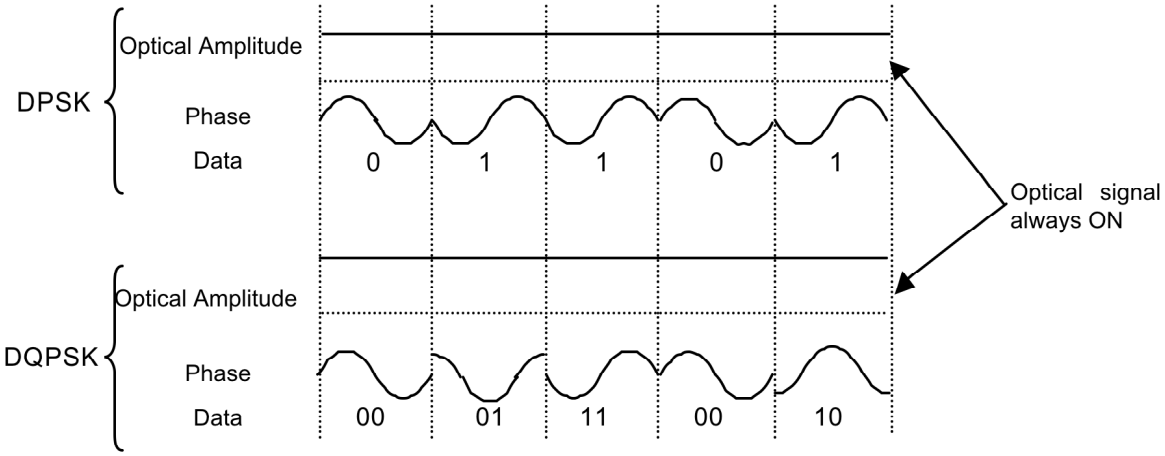

Figure 4. DPSK and DQPSK Transmissions

The amplitude and phase modulation methods are both illustrated below.

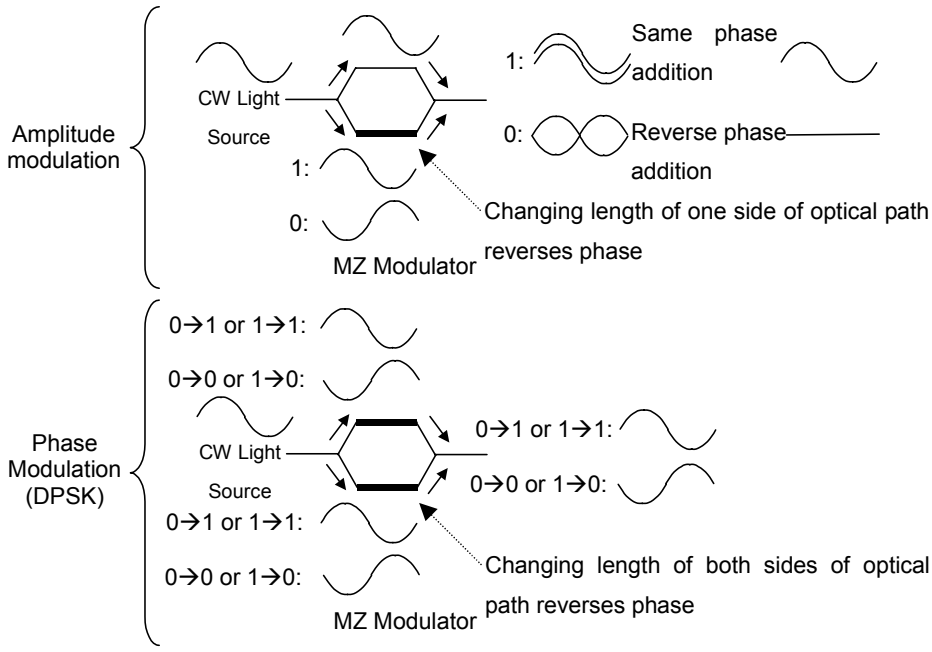

Figure 5. Amplitude and Phase Modulation

In the amplitude modulation method, a voltage is impressed only on one side of an MZ modulator to change the optical path length to a half cycle and ON or OFF occurs at the point where the waveforms of both sides are combined. On the other hand, in the phase shifting method, the phase of the output is reversed by changing both optical paths of the MZ modulator.
When sending data using the DPSK method, the 0/1 change of the data to transfer must be encoded in the data as shown below.

Transfer Data Change	Phase Change of Transfer Data
0 → 0	reversed
0 → 1	non-reversed
1 → 0	reversed
1 → 1	non-reversed

Encoding at the transmitter side is performed using a Pre-Coder; decoding is performed at the receiver side by the MZ modulator with added 1-bit delay to convert the phase modulation to amplitude modulation.

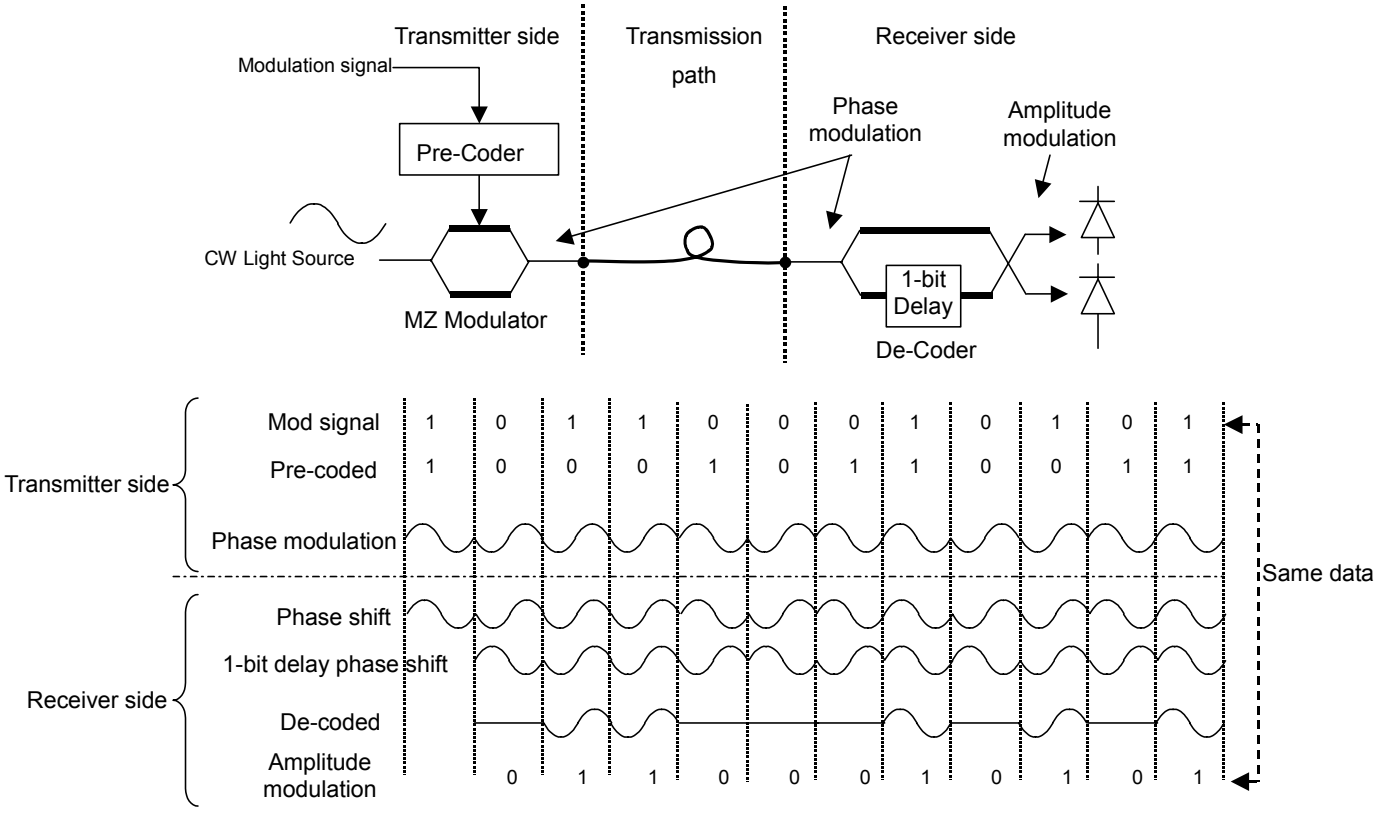

Figure 6. DPSK Transmission Circuit and Data Decoding

For long haul transmission, as described previously, there is active R&D into DQPSK and DP-QPSK methods with the aim of maintaining the data rate using modulation while decreasing symbol rate, and suppressing chromatic dispersion (CD) and polarization mode dispersion (PMD).

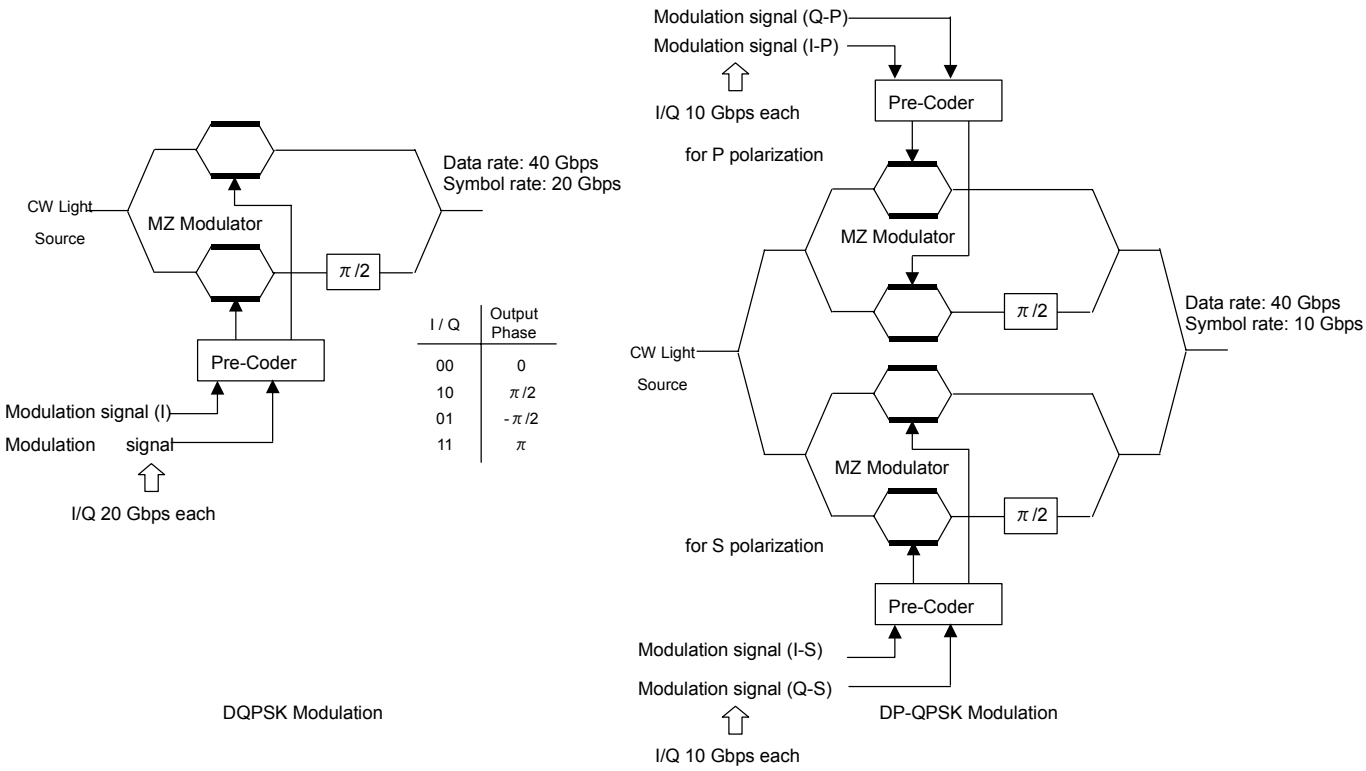

Figure 7. DQPSK, DP-QPSK Transmission Circuits

At 40G DQPSK, the symbol rate decreases to half the data rate because a 20-Gbps modulation signal is used for each of the two I and Q systems. The DP-QPSK scheme applies modulation to the two I and Q systems for both the P and S modulation waves and uses a 10-Gbps signal as each modulation signal. Although the data rate is fixed for DPSK, DQPSK, and DP-QPSK, the decreasing symbol rate from former to latter is an advantage, but conversely, the increase in the circuit complexity is a disadvantage.

4. Modulation Methods and Measurement Requirements Supporting 40/100GbE Standards

4.1 Measuring Modulation

Testing phase modulation transmissions in the previously described circuit requires confirmation of the Pre-Coder logic operation and phase modulation signal skew tolerance.

The Pre-Coder logic operation is described first.

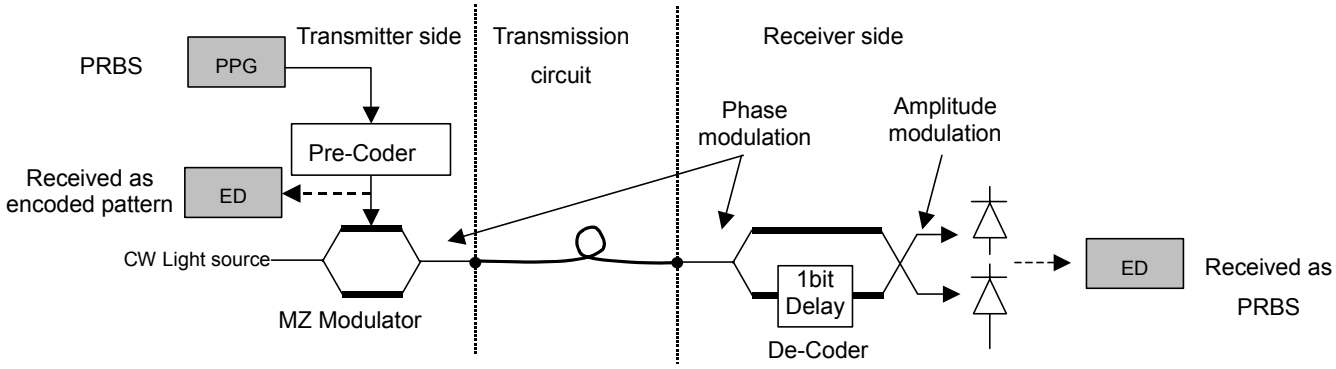

Figure 8. Pre-Coder Test System

The output of the pattern generator, such as a PRBS pattern, is input to the Pre-Coder as the modulation signal; the Pre-Coder output and assumed pattern are set as the receive pattern at the Error Detector side and checked by measuring the BER. To perform this test, not only is a BERTS function and ability to generate a pure PRBS pattern required, it is also necessary to have either a user programmable pattern with a high degree of freedom for easy setting of the Pre-Coder signal corresponding to the PRBS signal pattern length, or to have functions for generating and analyzing the pre-coded signal directly.

Usually, setting the programmable pattern at the BERTS requires the length of the actually used pattern and the length of the least common denominator of the programmable pattern setting resolution. For example, the PRBS pattern has a length of 2^n-1 bits and when the PRBS pattern is 2^{23}-1, the pattern length is 8,388,607 bits. When the programmable pattern length setting resolution is 1 bit, that length can be set as the pattern length, but if the setting resolution changes with pattern length as in a conventional BERTS, pattern setting becomes very inconvenient due to setting coarseness. For example, when the resolution is 128 bits, a pattern length of about 1 Gbit is required at the BERTS because 128 x 8,388,607 bit = about 1 Gbit. Each time the user shifts the same pattern by 1 bit, it is necessary to set 128 times on BERTS.

To solve this problem, Anritsu developed its MP1800 series offering programmable patterns with a high-df setting resolution whatever the pattern length, including 1 bit for a 10-Gbit/s band BERT, 2 bits for 20 Gbit/s, and 4 bits for 40 Gbit/s. In addition, Anritsu also provides software options to automatically generate and analyze DPSK, ODB, and DQPSK modulation signals without editing programmable patterns.

Phase modulation signal skew tolerance is described below.

At DQPSK and DP-QPSK tests, in addition to the Pre-Coder test described for the DPSK scheme, it is also necessary to test the I/Q signal skew tolerance. Since two signals are required for one meaning in a two I/Q modulation signal system, the timing of each signal must be synchronized. In addition, the effect of differences in the length of the two signal paths on modulation error in the transmission signal must also be considered.

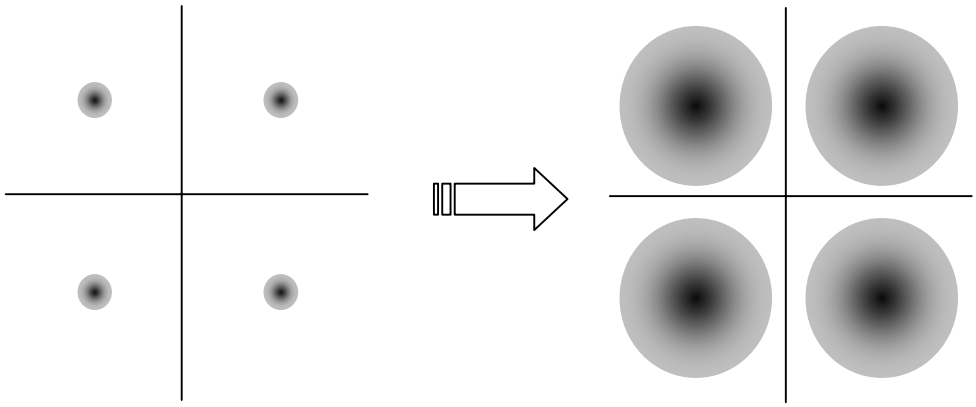

Figure 9. Modulation Error Outline

A 10-Gbps signal has a 1-bit cycle of 100 ps, which is equivalent to a path length of about 2 cm. In other words, when there is a difference in path lengths of about 1 cm, a 1-bit signal shows a tendency to skew, making path length design very important. At 20 Gbps, the 1-bit cycle is 50 ps, which is half the previous value and equivalent to a path length of 1 cm, requiring very accurate circuit design.
The following diagrams show the modulation measurement system required for DQPSK and DP-QPSK schemes.

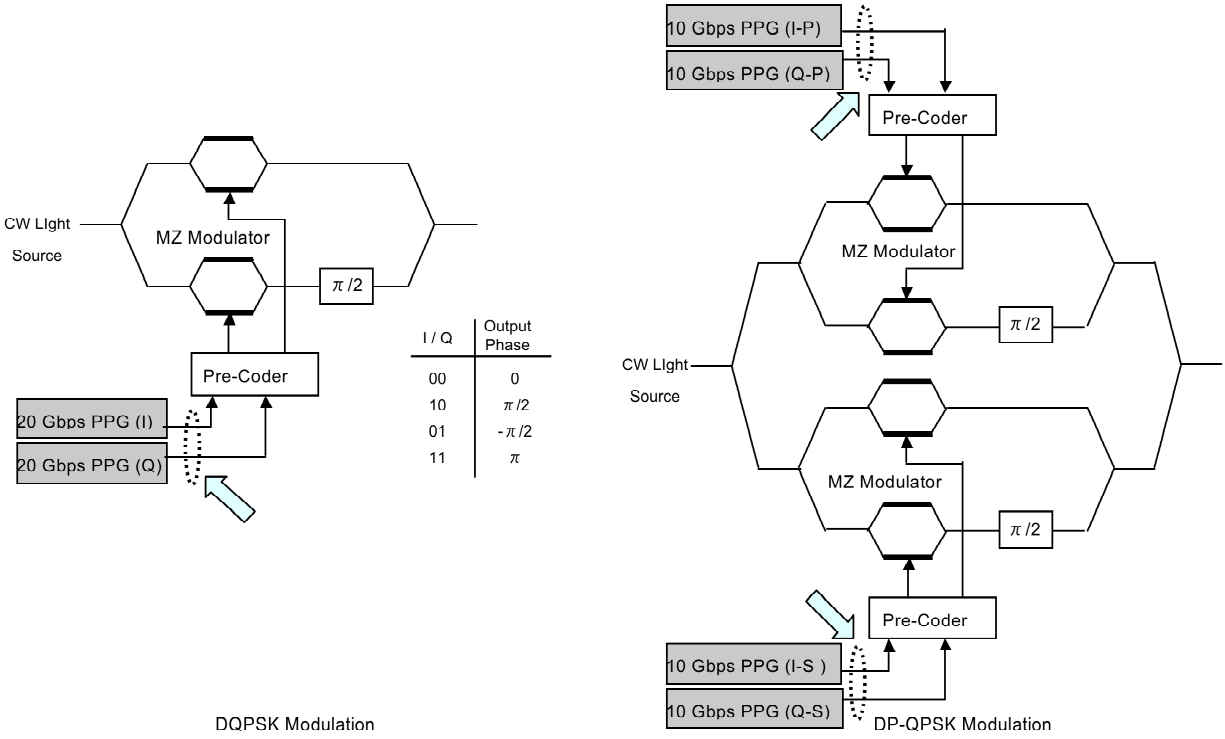

Figure 10. DQPSK, DP-QPSK Modulation Signal Test Systems

In Figure 10, as the minimum conditions, each I/Q test signal (surrounded by dotted oval) is not only at the same frequency but the bit pattern generation timing is also synchronized. Moreover, it is essential to assure the tolerance of the receive side to modulation error caused by drift in the generation timing of each I/Q signal by using the highest quality design standards.

4.2 40/100GbE Measurements

This section describes PMD, PMA and the equipment-side PCS (previously called “Multi Lane Distribution (MLD)”) interface as important issues in evaluation.

4.2.1 PMD Evaluation

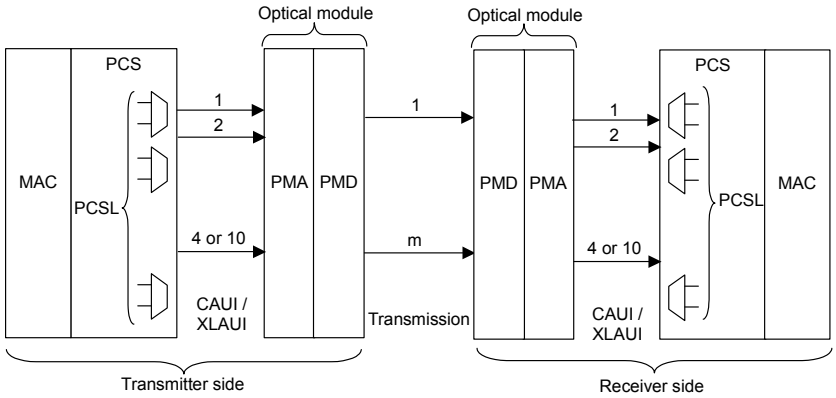

Figure 11. System Configuration (One Direction Only)

The appearance of PMD at 100 GbE in systems using 850 nm, 10 Gbps x 10 ch, and 1310 nm, 25.78 Gbps x 4 λ is a topic of vigorous discussion and many carriers are aiming to develop transmissions over distances of 10 km or more using 25.78 Gbps x 4 λ . When evaluating PMD, the light source in the measurement system requires much better Tr/Tf and Tj characteristics than the PMD so that there is no impact on the PMD output waveform. Recently, IEEE802.3ba and OIF have recommended values of 20 ps for Tr/Tf and 10 ps for Tj of the EML output waveform. However, since an EML generally has non-linear extinction characteristics for electrical input signals, when the crosspoint of such signals is at 50%, the crosspoint of the optical output waveform drifts to the 0 side and the waveform tends to become distorted. As a consequence, the light source for EML evaluation requires a crosspoint adjustment function allowing the optimum optical output waveform to be obtained.

4.2.2 PMA Evaluation

The SERDES function connecting the PMD and equipment side defines the PMA. Since the 4:1 SERDES used in 40G systems and the 10:4 SERDES used at 100G have lane number and bit rate conversion functions, they are called a Gear Box. This section describes issues with PMA evaluation. When performing transmission between multiple lanes, the most important issue to consider is evaluation of skew between lanes. Skew is caused by various factors such as transmission path propagation delay, fiber length, PCB pattern length, cable length, and IC propagation time delay. OIF recommends use of a Deskew function as defined in SFI-5P1 and SFI-5P2 as the interface at the electrical side of the 40-Gbps transponder for adjusting skew between multiple lanes. In SFI-5, a dedicated lane called Deskew is arranged alongside the data lanes to adjust the skew. However, designs for 40G XLAUI (10 Gbps x 4 lanes) and 100G CAUI (10 Gbps x 10 lanes) systems have no dedicated Deskew lane and instead use a procedure whereby data called the "Alignment Marker" for skew adjustment is embedded in the lanes.

At 100GbE, the CAUI 10-lane signal is split into 20 Physical Coding Sub-layer lanes (PCSLs) inside of equipment that have no physical interface. 20 PCSLs are used because although various numbers of 100 GbE lines, such as 1, 2, 4, 5, and 10 can be used, 20 is determined by the least common denominator required to assure the same processing at the device side. The Alignment Marker is sent over these 20 PCSLs by generating a 66-bit block 16,384 times to align the data skew in each lane.

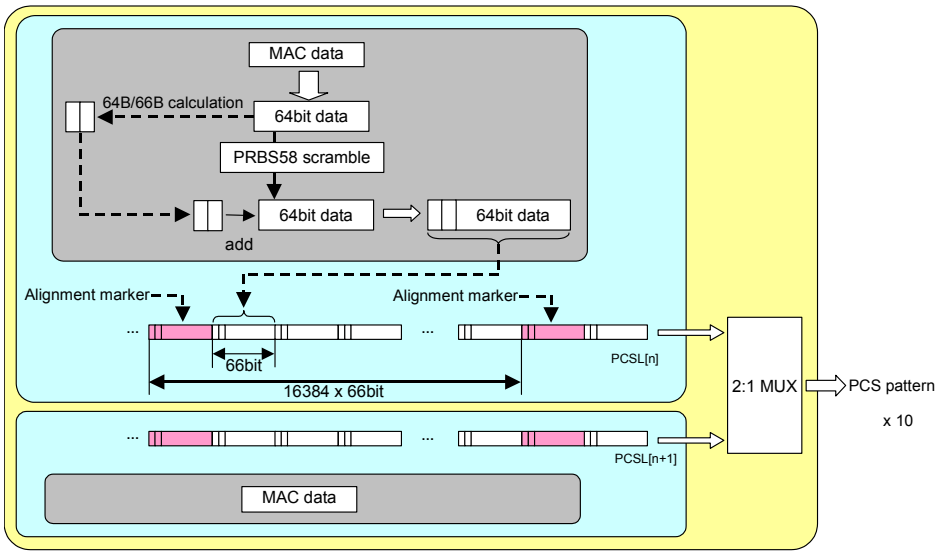

Figure 12. Alignment Marker Generation Outline

Since scrambling is not performed on the Alignment Marker, the DC balance must be maintained. Consequently, the first two bits are 01 and the following 32 bits are a PRBS58-generated sequence; the next 32 bits are the reverse of the previous 32 bits, maintaining the DC balance.

PCSL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Bit Number																				
59 – 66	~F4	~17	~B0	~10	~0B	~50	~15	~FA	~DF	~38	~DE	~B8	~CD	~AB	~B5	~EB	~30	~35	~6F	~E9
51 – 58	~21	~8E	~E8	~7B	~09	~C2	~26	~66	~76	~FB	~99	~55	~B2	~BD	~CA	~CD	~4C	~B7	~2A	~E5
43 – 50	~68	~71	~4B	~95	~07	~14	~4A	~45	~24	~C9	~6C	~91	~B9	~F8	~C7	~36	~31	~D6	~66	~F0
35 – 42	~C1	~9D	~59	~4D	~F5	~DD	~9A	~7B	~A0	~68	~FD	~B9	~5C	~1A	~83	~35	~C4	~AD	~5F	~C0
27 – 34	F4	17	B0	10	0B	50	15	FA	DF	38	DE	B8	CD	AB	B5	EB	30	35	6F	E9
19 – 26	21	8E	E8	7B	9	C2	26	66	76	FB	99	55	B2	BD	CA	CD	4C	B7	2A	E5
11 – 18	68	71	4B	95	7	14	4A	45	24	C9	6C	91	B9	F8	C7	36	31	D6	66	F0
3 – 10	C1	9D	59	4D	F5	DD	9A	7B	A0	68	FD	B9	5C	1A	83	35	C4	AD	5F	C0
2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 13. 100 GbE Alignment Marker

In a 100GbE 10:4 PMA, the MUX/DEMUX sequence is as follows:

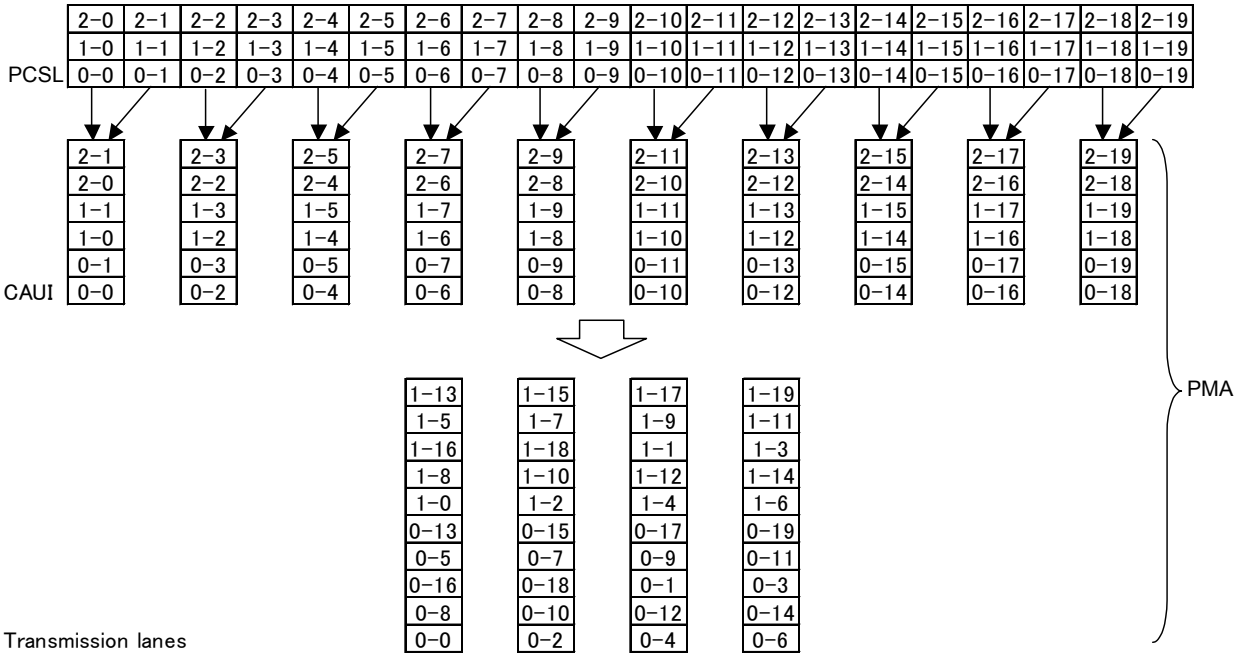

Figure 14. Bit Sequence

The CAUI is a physical electrical interface connecting the PMA and PCS at 10G x 10 lanes. The CAUI is MUXed to 25G x 4 lanes by the PMA and the signal is sent to the transmission circuit via the PMD. This process is reversed at the receive side.
At 100GbE, the lane is changed in the final stage where the appropriate bit appears due to the occurrence of bit skew. For example, when bit skew occurs in the transmission circuit where the worst jitter occurs easily, the skew appears as a 4 x n bit drift in the CAUI lane.

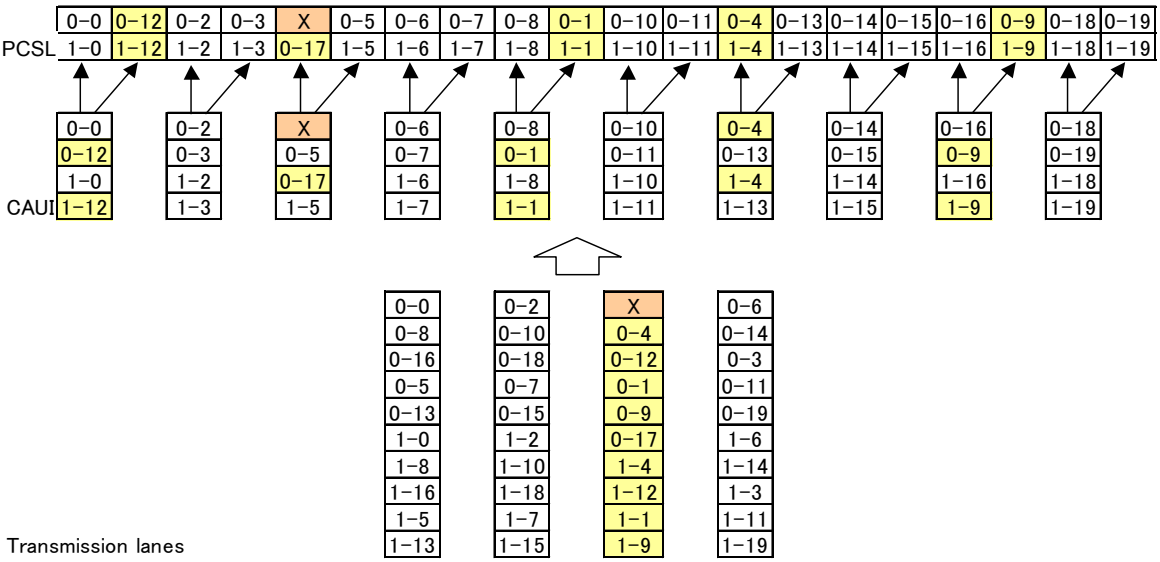

Figure 15. Skew between Transmission Lane and Device

On the other hand, when skew occurs at the transmission lane side of the CAUI due to differences in the length of traces on the optical-module PCB where the PMA is mounted or to differences in the buffer propagation time delay, it appears as shown below.

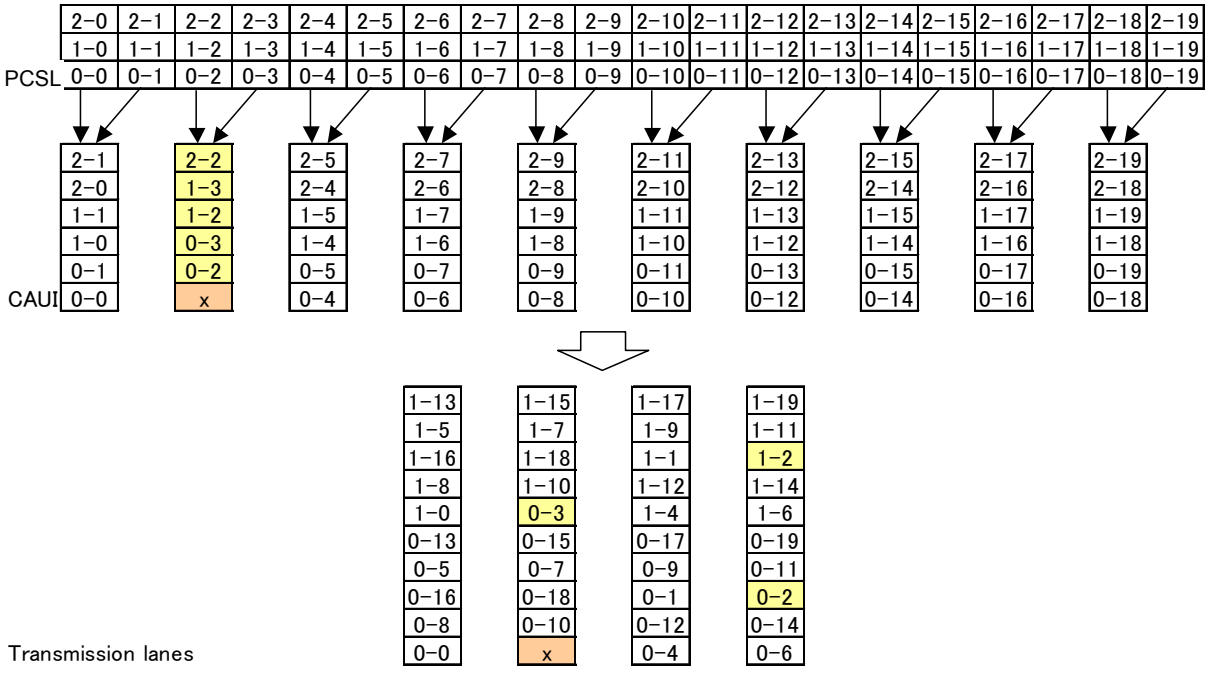

Figure 16. Skew between Device and Transmission Lane

The FIFO mounted on the PMA buffers jitter occurring in the transmission path but there is no function for correcting skew itself. As a result, the objective of the PMA test is not to test skew buffering, but is to confirm whether the bit width conversion occurs logically, requiring the following test.
Most importantly, not only are both sides of 10:4 tested but an independent pattern generator is required for the 10 lanes and 4 lanes. This is an important technique in reducing measurement cost. In other words, at input to the

10-lane and 4-lane sides, if the input timing is known, the output pattern is known too. Consequently, the key point for an instrument used to make these measurements is the ability to control the timing of the bit patterns generated by multiple PPGs. If this timing is uncertain, it is not possible to confirm the correct bit width conversion. The following figure shows the recommended measurement setup.

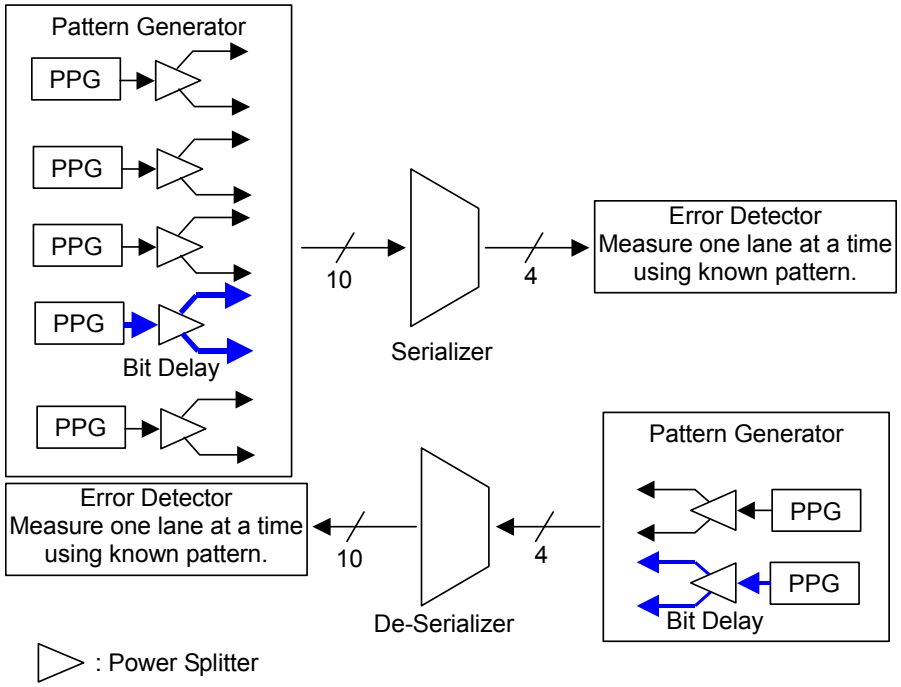

Figure 17. PMA Skew Test System

4.2.3 PCS Evaluation

The following test setup is used to evaluate the PCS at the device side when skew occurs in one lane of four lanes at the Transmission side as shown in Fig. 15 with skew from the transmission lane to device side, considering the spread of its impact on five lanes of the PCSL.

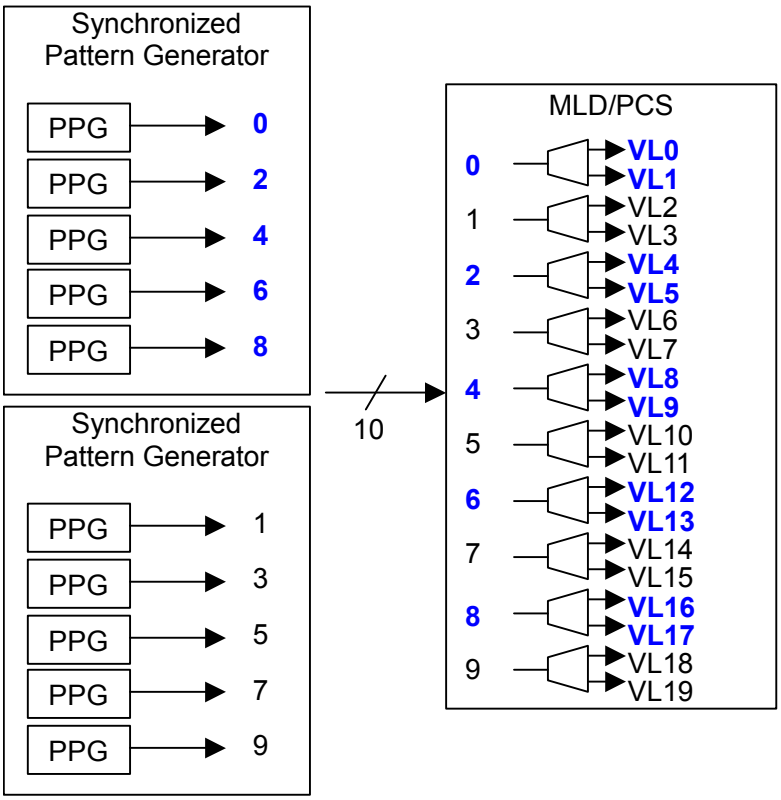

Figure 18. PCS Skew Test System

The PCS pattern including the odd or even alignment word emulating the skew generated at one lane of the CAUI is set at the PPG. Another key setting requirement is synchronizing the timing of the five PPGs. For example, as shown in Fig. 15, inputting the pattern for each one lane from the left of the CAUI lane for the skew from the transmission lane to the device to the PCS confirms the skew alignment function of the relevant PCSL.

5. Summary

This article explains some trends in ultra-high-speed transmission, such as the latest advances on 40 GbE long-distance transmissions and 100 GbE. It also describes evaluation issues and test systems from the perspective of a measuring instrument manufacturer.

In the future, Anritsu plans to continue offering customers even better measurement solutions for assuring the quality of their products and services.

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Anritsu

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Anritsu Corporation
5-1-1 Onna, Atsugi-shi, Kanagawa, 243-8555 Japan
Phone: +81-46-223-1111
Fax: +81-46-296-1264

• U.S.A.
Anritsu Company
1155 East Collins Blvd., Suite 100, Richardson,
TX 75081, U.S.A.
Toll Free: 1-800-267-4878
Phone: +1-972-644-1777
Fax: +1-972-671-1877

• Canada
Anritsu Electronics Ltd.
700 Silver Seven Road, Suite 120, Kanata,
Ontario K2V 1C3, Canada
Phone: +1-613-591-2003
Fax: +1-613-591-1006

• Brazil
Anritsu Eletrônica Ltda.
Praca Amadeu Amaral, 27 - 1 Andar
01327-010-Paraiso-São Paulo-Brazil
Phone: +55-11-3283-2511
Fax: +55-11-3288-6940

• Mexico
Anritsu Company, S.A. de C.V.
Av. Ejército Nacional No. 579 Piso 9, Col. Granada
11520 México, D.F., México
Phone: +52-55-1101-2370
Fax: +52-55-5254-3147

• U.K.
Anritsu EMEA Ltd.
200 Capability Green, Luton, Bedfordshire, LU1 3LU, U.K.
Phone: +44-1582-433200
Fax: +44-1582-731303

• France
Anritsu S.A.
16/18 avenue du Québec-SILIC 720
91961 COURTABOEUF CEDEX, France
Phone: +33-1-60-92-15-50
Fax: +33-1-64-46-10-65

• Germany
Anritsu GmbH
Nemetschek Haus, Konrad-Zuse-Platz 1
81829 München, Germany
Phone: +49-89-442308-0
Fax: +49-89-442308-55

• Italy
Anritsu S.p.A.
Via Elio Vittorini 129, 00144 Roma, Italy
Phone: +39-6-509-9711
Fax: +39-6-502-2425

• Sweden
Anritsu AB
Borgafjordsgatan 13, 164 40 KISTA, Sweden
Phone: +46-8-534-707-00
Fax: +46-8-534-707-30

• Finland
Anritsu AB
Teknobulevardi 3-5, FI-01530 VANTAA, Finland
Phone: +358-20-741-8100
Fax: +358-20-741-8111

• Denmark
Anritsu A/S
Kirkebjerg Allé 90, DK-2605 Brøndby, Denmark
Phone: +45-72112200
Fax: +45-72112210

• Spain
Anritsu EMEA Ltd.
Oficina de Representación en España
Edificio Veganova
Avda de la Vega, n° 1 (edf 8, pl 1, of 8)
28108 ALCOBENDAS - Madrid, Spain
Phone: +34-914905761
Fax: +34-914905762

• Russia
Anritsu EMEA Ltd.
Representation Office in Russia
Tverskaya str. 16/2, bld. 1, 7th floor.
Russia, 125009, Moscow
Phone: +7-495-363-1694
Fax: +7-495-935-8962

• United Arab Emirates
Anritsu EMEA Ltd.
Dubai Liaison Office
P O Box 500413 - Dubai Internet City
Al Thuraya Building, Tower 1, Suit 701, 7th Floor
Dubai, United Arab Emirates
Phone: +971-4-3670352
Fax: +971-4-3688460

• Singapore
Anritsu Pte. Ltd.
60 Alexandra Terrace, #02-08, The Comtech (Lobby A)
Singapore 118502
Phone: +65-6282-2400
Fax: +65-6282-2533

• India
Anritsu Pte. Ltd.
India Branch Office
3rd Floor, Shri Lakshminarayan Niwas, #2726, 80 ft Road,
HAL 3rd Stage, Bangalore - 560 075, India
Phone: +91-80-4058-1300
Fax: +91-80-4058-1301

• P.R. China (Hong Kong)
Anritsu Company Ltd.
Units 4 & 5, 28th Floor, Greenfield Tower, Concordia Plaza,
No. 1 Science Museum Road, Tsim Sha Tsui East,
Kowloon, Hong Kong
Phone: +852-2301-4980
Fax: +852-2301-3545

• P.R. China (Beijing)
Anritsu Company Ltd.
Beijing Representative Office
Room 2008, Beijing Fortune Building,
No. 5, Dong-San-Huan Bei Road,
Chao-Yang District, Beijing 100004, P.R. China
Phone: +86-10-6590-9230
Fax: +86-10-6590-9235

• Korea
Anritsu Corporation, Ltd.
8F Hyunjuk Building, 832-41, Yeoksam Dong,
Kangnam-ku, Seoul, 135-080, Korea
Phone: +82-2-553-6603
Fax: +82-2-553-6604

• Australia
Anritsu Pty. Ltd.
Unit 21/270 Ferntree Gully Road, Notting Hill,
Victoria 3168, Australia
Phone: +61-3-9558-8177
Fax: +61-3-9558-8255

• Taiwan
Anritsu Company Inc.
7F, No. 316, Sec. 1, Neihu Rd., Taipei 114, Taiwan
Phone: +886-2-8751-1816
Fax: +886-2-8751-1817

Please Contact:

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